|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1.** | | The \_\_\_\_\_\_ format is usually used to store data . | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | BCD \* | | | | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | Decimal | | | | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | Hecadecimal | | | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | Octal | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1. A source program is usually in \_\_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | Assembly language | | | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | Machine level language | | | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | High-level language\* | | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | Natural language | | | | | | | | | | | | | | | | | | | | | | | | |
| 3. | | Which memory device is generally made of semi-conductors ? | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | RAM \* | | | | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | Hard-disk | | | | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | Floppy disk | | | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | Cd disk | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4.The small extremely fast, RAM’s are called as \_\_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | Cache\* | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | Heaps | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | Accumulators | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | Stacks | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5.The ALU makes use of \_\_\_\_\_\_\_ to store the intermediate results . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | Accumulators\* | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | Registers | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | Heap | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | Stack | | | | | | | | | | | | | |
| 6.The control unit controls other units by generating \_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | Control signals | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | Timing signals\* | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | Transfer signals | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | Command Signals | | | | | | | | | | | | | | | | | | | | | |
| 7.\_\_\_\_\_\_ are numbers and encoded characters, generally used as operands . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Input | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Data\* | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Information | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Stored Values | | | | | | | | | | | | | | | | | | |
| 8.\_\_\_\_\_\_ bus structure is usually used to connect I/O devices . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | Single\* | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | Multiple | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | Star | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | Ra | | | | | | | | | | | |
| 9.The I/O interface required to connect the I/O device to the bus consists of \_\_\_\_\_\_ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Address decoder and registers | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Control circuits | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Both a and b\* | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Only b | | | | | | | | | | | | | | | | | | |
| 10.To reduce the memory access time we generally make use of \_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Heaps | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Higher capacity RAM’s | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | SDRAM’s | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Cache’s\* | | | | | | | | | | | | | | | | | | | |
| 1. \_\_\_\_\_ is generally used to increase the apparent size of physical memory . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | Secondary memory | | | | | | | | | | | |
| **b.** | | | | | | | | Virtual memory\* | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Hard-disk | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Disks | | | | | | | | | | | | | | | | | | | |
| 12.MFC stands for | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Memory Format Caches. | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Memory Function Complete.\* | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Memory Find Command. | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Mass Format Command. | | | | | | | | | | | | | | | | | | | |
| 13.The time delay between two successive initiation of memory operation \_\_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | Memory access time | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | Memory search time | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | Memory cycle time\* | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | Instruction delay | | | | | | | | |
| 14.The decoded instruction is stored in \_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | IR\* | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | PC | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Registers | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | MDR | | | | | | | | | | | | | | | | | | | |
| 15.During the execution of a program which gets initialized first ? | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | MDR | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | IR | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | PC\* | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | MAR | | | | | | | | | | | | | | | | | | |
| 16.Which of the register/s of the processor is/are connected to Memory Bus ? | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | PC | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | | MAR\* | | | | | | |
| **c.** | | | | | | | | | IR | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Both a and b | | | | | | | | | | | | | | | | | | |
| 17.ISP stands for, | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Instruction Set Processor\* | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Information Standard Processing | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Interchange Standard Protocol | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Interrupt Service Procedure | | | | | | | | | | | | | | | | | | |
| 18.The internal Components of the processor are connected by \_\_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | Processor intra-connectivity circuitry | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | Processor bus\* | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | Memory bus | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | Rambus | | | | | | | | | | | |
| 19.\_\_\_\_\_ is used to choose between increment the PC or performing ALU operations . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Conditional codes | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Multiplexer\* | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Control unit | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | None of these | | | | | | | | | | | | | | | | | | |
| 20.The registers, ALU and the interconnection between them are collectively called as \_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | Process route | | | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | Information trail | | | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | Information path | | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | Data path\* | | | | | | | | | | | | | | | | | | | | | | | | |
| 21.During the execution of the instructions, a copy of the instructions is placed in the \_\_\_\_\_\_ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | Register | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | RAM | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | System heap | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | Cache\* | | | | | | | | | | | | | | | | |
| 22.Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster ? | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | A\* | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | B | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Both take the same time | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Insuffient information | | | | | | | | | | | | | | | | | | | |
| 23.A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Super-scaling | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Pipe-lining\* | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Parallel Computation | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | None of these | | | | | | | | | | | | | | | | | | |
| 24.The clock rate of the processor can be improved by | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | Improving the IC technology of the logic circuits | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | Reducing the amount of processing done in one step | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | By using overclocking method | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | All of the above\* | | | | | | | | | | | |
| 25.An optimizing Compiler does, | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | Better compilation of the given piece of code. | | | | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | Takes advantage of the type of processor and reduces its process time. | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | Does better memory management. | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | Both a and c | | | | | | | | | | | | | | | | | | | | | |
| 26.SPEC stands for, | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Standard Performance Evaluation Code. | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | System Processing Enhancing Code. | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | System Performance Evaluation Corporation. | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | Standard Processing Enhancement Corporation. | | | | | | |
| 27.When Performing a looping operation, the instruction gets stored in the \_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Registers | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | Cache | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | System Heap | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | System stack | | | | | | | | | | | | | | | | | | |
| 28.CISC stands for | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | Complete Instruction Sequential Compilation | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | Computer Integrated Sequential Compiler | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | | | | | Complex Instruction Set Computer | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | Complex Instruction Sequential Compilation | | | | | | | | | | | |
| 29.The different modes of operation of a computer is | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | User and System mode | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | User and Supervisor mode | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Supervisor and Trace mode | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Supervisor,User and Trace mode | | | | | | | | | | | | | | | | | | |
| 30.If the instruction, Add R1,R2,R3 is executed in a system which is pipe-lined, then the value of S is (Where S is term of the Basic performance equation) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | 3 | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | ~2 | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | | | ~1 | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | 6 | | | | | | | | | | | | | |
| 31.The instructions which can be run only supervisor mode are | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | Non-privileged instructions | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | System instructions | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | | | | | Privileged instructions | | | | | | | | | | | |
| **d.** | | | | | | | | | Exception instructions | | | | | | | | | | | | | | | | | | |
| 32.A privilege exception is raised, | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | When a process tries to change the mode of the system | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | When a process tries to change the piority level of the other processes | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | When a process tries to access the memory allocated to other user | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | All of the above\* | | | | | | | | | | | | | | | | | | | | | |
| 33.How is a privilege exception dealt ? | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | The program is alted and the system switches into supervisor mode and restarts the program execution | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | The Program is stopped and removed from the queue | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | The system switches the mode and starts the execution of a new process | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | The system switches mode and runs the debugger | | | | | | | | | | | | | | | | | | | |
| 34.After reset, CPU begins execution of instruction from memory address | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | 0101H | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | 8000H | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | 0000H | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | FFFFH | | | | | | | | | | | | | | | | | | |
| 35.Synchronous means \_\_\_\_\_\_\_ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | At irregular intervals | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | | | At same time | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | | | | At variable time | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | | None of these | | | | | |
| 36.Synchronous means \_\_\_\_\_\_\_ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | At irregular intervals | | | | | | | | | | | |
| **b.\*** | | | | | | | | | | | | | | | | At same time | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | At variable time | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | None of these | | | | | | | | | | | |
| 37.When CPU is executing a Program that is part of the Operating System, it is said to be in | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Interrupt mode | | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | System mode | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Half mode | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Simplex mode | | | | | | | | | | | | | | | | | | | |
| 38.IC chips based on packaging density are | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Small-Scale Integration (SSI): Up to 12 gates | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Medium-Scale Integration (MSI): 12–99 gates | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Small- Scale Integration (SSI): Up to 14 gates | | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | Both a and b | | | | | | | | | | | | | | | | | | | |
| 39.In a sequential memory, the words are stored in and out in a sequence. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Write | | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | Read | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Write/Read | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | All of the above | | | | | | | | | | | | | | | | | | | |
| 40.A memory stores data for processing and the instructions for \_\_\_\_\_\_\_\_\_. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | Result | | | | | |
| **b.\*** | | | | | | | | | | | | | | | | | | | | | | Execution | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | | | | Progress | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | | All of the above | | | | | |
| 41.Number of stored bits per unit area, which determines overall storage capacity and memory cost per bit. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | | | | Area Efficiency | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | | Access Time | | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | | | Power Consumption | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | None of the above | | | | | | |
| 42.The \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ of the desired memory location is applied to the address input terminals. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | Name | | |
| **b.\*** | | | | | | | | | | | | | | | | | | | | | | | | | Address | | |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | Number | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | Level | | |
| 43.In a sequential memory, the words are stored in and read out in a\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ . | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | Parallel | | | | | |
| **b.\*** | | | | | | | | | | | | | | | | | | | | | | Sequence | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | | | | Length | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | | None of the above | | | | | |
| 44.I/O function allows to exchange data directly between an | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | Process States | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | Registers | | | |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | | | | I/O module and the processor | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | I/O devices | | | |
| 45.Cache memory is intended to provide memory access | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | Fastest | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Slow | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Very Slow | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Fast | | | | | | | | | | | | | | | | | | | |
| 46.Data stores in | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | Monitor | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | | Mouse | | | | | | |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | secondary storage | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | Keyboard | | | | | | |
| 47.Interrupts are provided primarily as a way to | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | | | | Improve processor utilization | | | | | | |
| **b.** | | | | | | | | | Improve processor execution | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Improve processor control | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Improve processor speed | | | | | | | | | | | | | | | | | | |
| 48.Index register involves adding an | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | Index | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | Instruction | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | Information | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | I/O device | | | | | | | | | | | | | | | | |
| 49.Program counter contains the address of the | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Next programs to be fetched | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Previous programs to be fetched | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Previous information to be fetched | | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | Next information to be fetched | | | | | | | | | | | | | | | | | | | |
| 50.Memory modules consist of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | Set of Instructions | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | | Set of Registers | | | | | | |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | Set of Locations | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | Set of Programs | | | | | | |
| 51.Processor is often referred to | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | | Central Processing Unit | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | Hardware | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | System Bus | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | I/O Modules | | | | | | | | |
| 52.Segment pointers divided memory into | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Register | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Process | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | Segments | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Scaling | | | | | | | | | | | | | | | | | | | |
| 53.The set of all logical addresses generated by a program is referred to as a | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | Memory Addresses | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | Physical Addresses | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | | | Logical address Space | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | Buffer Addresses | | | | | | | | | | | | | |
| 54.Instruction register contains the instructions most | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | recently deleted | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | Recently fetched | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Recently updated | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Recently executed | | | | | | | | | | | | | | | | | | |
| 55.The unit of data exchange between cache and main memory is known as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Cache Memory | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Cache Size | | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | Block Size | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Mapping Function | | | | | | | | | | | | | | | | | | | |
| 56.Address registers contain main memory addresses of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Scheduling | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Registers | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Protocols | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | Data and instruction | | | | | | | | | | | | | | | | | | |
| 57.Stack pointer is a register that points to the | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Pop the stack | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Push the stack | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | Top of the stack | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | Bottom of the stack | | | | |
| 58.Cache size issue can have significant impact on | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | input | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | output | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Information | | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | Performance | | | | | | | | | | | | | | | | | | | |
| 59.In data processing, processor perform some | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Arithmetic or logic operation on information | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Arithmetic or logic operation on instruction | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Arithmetic or logic operation on programs | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | Arithmetic or logic operation on data | | | | | | | | | | | | | | | | | | |
| 60.Data and instructions that are being used frequently are stored in | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Cache | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | Block | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | hard disk | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | main memory | | | | | | | | | | | | | | | | | | |
| 61.PerformanceX = 1/ Execution Time x the given relation shows that | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | Performance is increased when execution time is decreased | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Performance is increased when execution time is increased | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Performance is decreased when execution time is decreased | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | None | | | | | | | | | | | | | | | | | | |
| 62.The processor having Clock cycle of 0.25ns will have the clock rate of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | 2GHz | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | 3GHz | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | 4GHz | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | 8GHz | | | | | | | | | | | | | | | | | | |
| 63.The valid and unimpeachable measurement of performance of any computer is | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Clock rate | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Instruction set | | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | Execution time | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Delay time | | | | | | | | | | | | | | | | | | | |
| 64.The native MIPS has the MIPS measurement of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | MIPS = Instruction count/(Execution time)10^6 | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | MIPS = Instruction count/(Execution time)10^3 | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | MIPS = Instruction count/Execution time | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | MIPS = (Execution time)10^6 | | | | | | | | | | | | | | | | | | | |
| 65.If computer A execute a program in 10 seconds and computer B runs the same in 15 seconds, how much faster is computer A than computer B | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | 1.4 times | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | 1.5 times | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | 1 time | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | 5.1 times | | | | | | | | | | | | | | | | | | |
| 66.For two computers X and Y, if the performance of computer X is greater than the performance of computer Y, we have | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | PerformanceX =2PerformanceX | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | PerformanceX =PerformanceX | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | PerformanceX < PerformanceY | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | | | | | PerformanceX > PerformanceY | | | | | | | | | | | | | | |
| 67.The total amount of work done during execution, in a given time is referred to as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Response time | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | Execution time | | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | Through put | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | Delay time | | | | | | | | | | | | | | | | | | | |
| 68.To increase the performance of the computer its through put is increased by | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | | | Replacing processor with faster version | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | | | Replacing input/output | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | | | Replacing Operating System | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | | | Replacing Cache | | | | | | | |
| 69.Computer A having clock cycle time of 250 ps and cycle per instruction of 2.0 for some programs, and computer B having clock cycle time of 500 ps and a cycle per instruction of 1.2 for the same program. Which one is faster for this program | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | Computer A | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Computer B | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Both will have same time | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | None of the above | | | | | | | | | | | | | | | | | | |
| 70.When the PC having Clock rate of 2 and the CPU clock cycle for a program is 4 then Execution time of this computer for a program will be | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | 1 | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | 1.5 | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | 1.75 | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | 2 | | | | | | | | | | | | | | | | | | |
| 71.The time between the start and the end of program execution is known as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | Response time | | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | Execution time | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | Delay time | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | both a and b | | | | | | | | | | | | | | | | | | | |
| 72.Computer B having execution time 110 ns and computer A having 1001 then | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | A is 9.1 times as fast as B for programs | | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | B is 9.1 times as fast as A for programs | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | A is 8 times as fast as B for programs | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | B is 8 times as fast as A for programs | | | | | | | | | | | | | | | | | | | |
| 73.A first goal of compiler writer | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | Correctness | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Fast performance | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | Callee saving | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Data dependence | | | | | | | | | | | | | | | | | | |
| 74.In 32-bit addressing mode, the address field is either 1 byte or | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | 2 bytes | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | 3 bytes | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | | 4 bytes | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | 5 bytes | | | | | | | | | | | | | | |
| 75.The operation is normally specified in one field, known as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | Oprand | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | | | | | | | Opcode | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | Operation | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | Instruction count | | | | | | | | | | | | |
| 76.The length of 80x86 instructions can vary between | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | 1 to 10 bytes | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | 2 to 8 bytes | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | 2 to 17 bytes | | | | | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | 1 to 17 bytes | | | | | | | | | | | | | | | | | | | | | | |
| 77.CPU provides enabling signals through | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | control bus | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | data bus | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | address bus | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | ordinary bus | | | | | | | | | | | | | | |
| 78.C=A+B in assembly language will be written as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | add AB | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | addition AB | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | add C, A,B | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | addition A,B | | | | | | | | | | | | | | | | |
| 79.In assembly languageC= A-B will be written as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | sub AB | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | subtraction AB | | | | | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | sub C, A,B | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | subtraction A,B | | | | | | | | | | | | | | | | | | | | | | |
| 80.In a computer, set of electrical paths which is used to transfer data is called | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | bus | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | monitors | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | computer clock | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | ports | | | | | | | | | | | | | | | | | | |
| 81.Computer bus which allows the processor to communicate with peripheral devices is | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | expansion bus | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | system bus | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | memory bus | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | processor bus | | | | | | | | | | | | | | | | | |
| 82.Computer address bus is | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | bidirectional | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | | unidirectional | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | multidirectional | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | circular | | | | | | | | | | | | | | | | | |
| 83.Computer bus with 64 lines can carry | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | 32bits | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | | 64bits | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | 16bits | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | 8bits | | | | | | | | | | | | | | | | | | | | |
| 84.Which of the following is not a type of bus in computer? | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | data bus | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | address bus | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | timer bus | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | control bus | | | | | | | | | | | | | | | | | |
| 85.Example of computer logic operation is | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | AND | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | OR | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | NOR | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | all of these | | | | | | | | | | | | | | | | | | |
| 86.Computer system mainly consists of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | CPU | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | main memory | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | I/O unit | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | | | | | | | all of these | | | | | | | | | | | | |
| 87.Basic unit of computer is | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | ALU | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | CU | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | I/O unit | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | all of these | | | | | | | | | | | | | | | | | | |
| 88.Most of time, computer instructions are divided into | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | function code | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | instruction code | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | operand | | | | | | | | | | | | | | | | | | |
| **d.\*** | | | | | | | | | both a and c | | | | | | | | | | | | | | | | | | |
| 89.Binary code which gives an actual instruction is called | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | instruction code | | | | | | | | | | | | | | | | | | | | | | | |
| **b.** | | | | logical code | | | | | | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | function code | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | address | | | | | | | | | | | | | | | | | | | | | | | |
| 90.In instruction format, address of any data location is said to be | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | function code | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | instruction code | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | | | | operand | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | logical code | | | | | | | | | | | | | | | |
| 91.Built-in set of machine code instructions of computer are called | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | instruction set | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | | transfer of data | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | | | logical operations | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | | | logical set | | | | | | | | | |
| 92.Two main types of branch instructions are | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | conditional branch | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | | unconditional branch | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | | logical branch | | | | | | | | | | |
| **d.\*** | | | | | | | | | | | | | | | | | both a and b | | | | | | | | | | |
| 93.Instructions that are programmed to make decisions are termed as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | branch instructions | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | programmed instructions | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | logical instructions | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | arithmetic instructions | | | | | | | | | | | | | | | | | | |
| 94.Branch instruction 'JUMP TO SUBORDINATE' is an example of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | unconditional branch | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | arithmetic branch | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | transferring branch | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | conditional branch | | | | | | | | | | | | | | | | | | |
| 95.Branch instruction 'JUMP IF ZERO' is an example of | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | transferring branch | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | | | | | | conditional branch | | | | | | | | | | | | | | | | | | |
| **c.** | | | | | | | | | unconditional branch | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | arithmetic branch | | | | | | | | | | | | | | | | | | |
| 96.Branch instruction is also known as | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | jump instruction | | | | | | | | | | | |
| **b.** | | | | | | | | | | | | | | | | logical instruction | | | | | | | | | | | |
| **c.** | | | | | | | | | | | | | | | | arithmetic instruction | | | | | | | | | | | |
| **d.** | | | | | | | | | | | | | | | | programmed instructions | | | | | | | | | | | |
| 97.…………… is a piece of hardware that executes a set of machine–language instructions. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | Controller | | | | | | | | | | | | | | | | | | |
| **b.** | | | | | | | | | Bus | | | | | | | | | | | | | | | | | | |
| **c.\*** | | | | | | | | | Processor | | | | | | | | | | | | | | | | | | |
| **d.** | | | | | | | | | Motherboard | | | | | | | | | | | | | | | | | | |
| 98.The computer performs all mathematical and logical operations inside it′s | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | Memory unit | | | | | | | | | | | | | | | | | | | | | | | |
| **b.\*** | | | | Central processing unit | | | | | | | | | | | | | | | | | | | | | | | |
| **c.** | | | | Output unit | | | | | | | | | | | | | | | | | | | | | | | |
| **d.** | | | | Visual display unit | | | | | | | | | | | | | | | | | | | | | | | |
| 99.Computer bus which moves data between the central processor and memory is called | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O bus |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | CPU bus |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | | processor bus |
| **d.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | data bus |
| 100.Compiler of the system, is an example of | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | System hardware |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | Input |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | System software |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | Output |
| 101.I/O interrupt-driven is more efficient than | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O Modules |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O Devices |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | Programmed I/O |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | CPU |
| 102.Data moved between computer components through | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O Processor |
| **b.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O Modules |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O Devices |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O Buffers |
| 103.I/O instruction Control is used to activate an | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | Interrupt driven I/O |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | Internal device |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | External device |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O devices |
| 104.I/O modules performs the requested action on | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | Programmed I/O |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | Direct Memory Access (DMA) |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | | Interrupt driven I/O |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O devices |
| 105.I/O instruction Transfer used to read the | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | Data |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | Information |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | | Instructions |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | Description |
| 106.I/O instruction Status tests various | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | Control Conditions |
| **b.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | Status conditions |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O device |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | Memory |
| rocessor-I/O involves data transferring between | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | Computers |
| **b.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | Processor and I/O modules |
| **c.** | | | | | | | | | | | | | | | | | | | | | | | | | | Registers |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | User Processes |
| 107.I/O function allows to exchange data directly between an | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **a.** | | | | | | | | | | | | | | | | | | | | | | | | | | Process States |
| **b.** | | | | | | | | | | | | | | | | | | | | | | | | | | Registers |
| **c.\*** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O module and the processor |
| **d.** | | | | | | | | | | | | | | | | | | | | | | | | | | I/O devices |